ABSTRACT OF THE DISCLOSURE

A memory device is provided. The memory device has a memory array and control circuitry to control operations to the memory array. A redundant register having a bit is also included. The bit is at a first level when two rows of the memory array are shorted together or at a second level when four rows of the memory array are shorted together. The control circuitry instructs an address counter, during an erase operation, to increment row addresses of the rows of the memory array by two rows when the bit is at the first level or four rows when the bit is at the second level.